Replacing the Cypress CY14B104LA-ZS/BA45xxx nvSRAM with Everspin's MR2A08AxYS/MA35xxx MRAM

GENERAL CONSIDERATIONS for REPLACING nvSRAM with MRAM

Every write with an MRAM is instantly non-volatile for at least 20 years. There is no transfer of data from a volatile to a non-volatile memory cell, no external capacitors or back up batteries. The elimination of external components, highly reliable data retention, and 35ns SRAM compatible READ/WRITE Access times make the Everspin MRAM a viable candidate for replacing the Cypress CY14B104LA-ZS/BAxxx nvSRAM without compromising system performance.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

MR2A08A COMPARISON TO CY14B104LA

The Everspin MRAM solution provides:

- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No Vcap or Vbatt required
- Immediate (<1ns) Power-off with no loss of data
- No complex Software STORE/RECALL routines
- Fast Start-up time (2ms vs. 20ms)
- Unlimited Read and Write cycles - No Wear-out Concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM

COMPATIBILITY

The Everspin MR2A08AxYS35 (44-TSOP2) and MR2A08AxMA35 (FBGA) memories are pin, timing, and package compatible with the Cypress CY14B104LA-ZS45xxx and CY14B104LA-BA45xxx nvSRAM's respectively.

TIMING COMPATIBILITY

Both Everspin MRAM and nvSRAM have standard, compatible asynchronous SRAM timing. The MRAM however, retains data even at power off for an indefinite period of time and over temperature cycling. With a 35 ns read/write cycle time, the MRAM is compatible with similar nvSRAM speed grade options.

It is important to note that the Everspin MR2A08Axxx device requires a minimum of 12ns hold time from Write Enable (and Chip Enable) high to Address invalid (Please see T_{WHAX}

and T_{EHAX} in the MR2A08A data sheet available here.) Most microprocessors can accommodate this Hold time.

PIN COMPATIBILITY

- 4Mb organized in the 512Kx8 configuration
- 3.3 volt nominal operation
- Standard SRAM parallel address pins (A0-18)
- Standard byte-wide, bidirectional data pins (DQ0-7)
- Standard control signals (/E, /W, /G)

The MR2A08A does not require an external capacitor and the other associated passive components required by the CY14B104LA-xx devices.

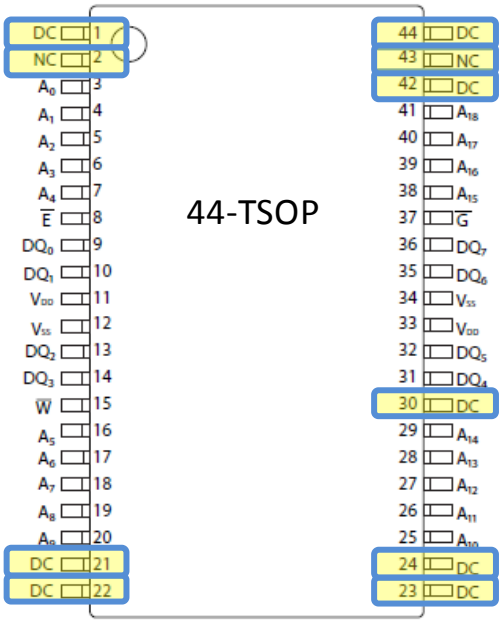
Tables 1 and 2 highlight the differences in signal name and function for the Everspin and Cypress components. The primary difference between the Cypress and Everspin devices are the two pins on the nvSRAM: VCAP and /HSB. These pins are used to support the nvSRAM backup cycle and are not required for operation of the MRAM.

V_{CAP} pin
A capacitor is required on the V_{CAP} pins (Pin 30 on the TSOP2 and Ball E3 on the FBGA) on nvSRAM devices. Everspin assigns a "Do not connect" (DC) to the corresponding pins on the MRAM. When replacing the Cypress nvSRAM with the Everspin MRAM, it is required that this pin be either left floating or pulled to V_{SS}.

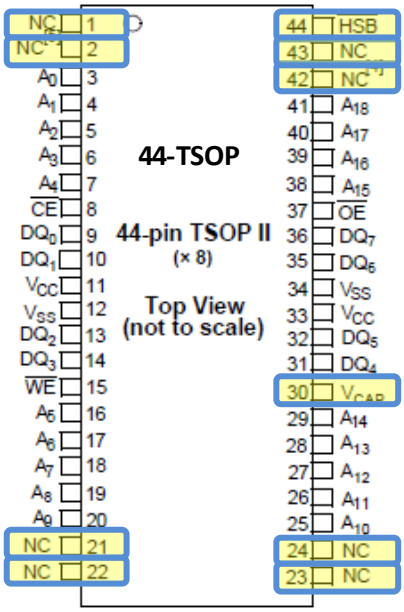
/HSB pin
The /HSB pin of the nvSRAM (Pin 44 of the TSOP2 and ball G2 on the FBGA) is used to either initiate a Hardware Store or indicate a Hardware Store is in process. The corresponding pin on the Everspin MRAM is labeled as "Do not connect" on the TSOP2 and "Not Connected" on the FBGA. Pin 44 on the Everspin TSOP2 device has an internal pull down and should not be pulled to any voltage other than V_{IL}. The G2 pin on the Everspin FBGA is Not Connected to the die. Therefore, a Host processor should not expect the MRAM to drive this pin to a particular voltage level.

Figure 1 - Pinout comparison between MRAM and nvSRAM, 44 pin TSOP2 package

Everspin



Cypress

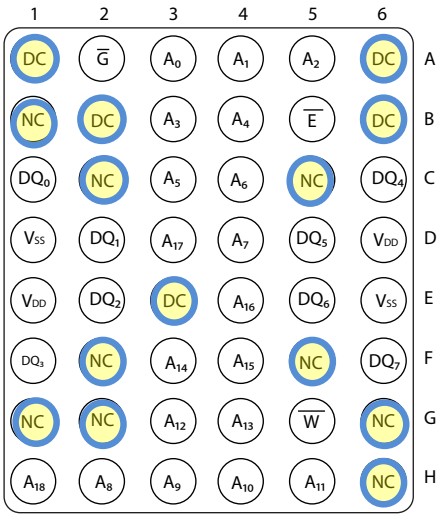


PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
1	DC	NC	Do not connect	Internally pulled down. Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
2	NC	NC	Not Connected to die	Do not Care
21	DC	NC	Do not connect	Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
22	DC	NC	Do not connect	Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
23	DC	NC	Do not connect	Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
24	DC	NC	Do not connect	Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
30	DC	VCap	Do not connect	Internal pull-down/Prefer to float. If not floating, must be kept at a Steady State to Vss to minimize current draw.
42	DC	NC	Do not connect	Internally pulled down. Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)
43	NC	NC	Not connected to die	Do not care.
44	DC	HSB_	Do not connect	Internally pulled down. Prefer to float. Acceptable to either Pull up/Pull down, however this pin must remain steady-state (VIH or VIL)

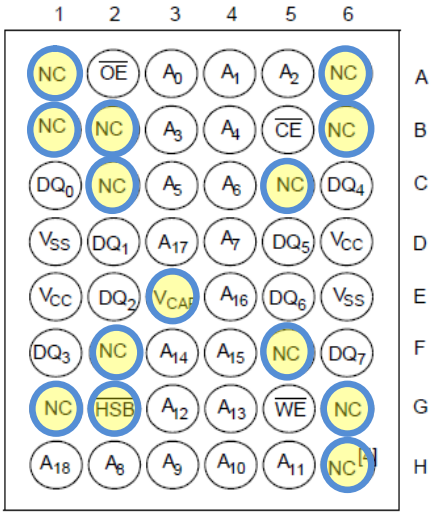
Table 1- Pin function comparison between MRAM and nvSRAM, 44 pin TSOP2 package

Figure 2 - Pinout comparison between MRAM and nvSRAM, 48 FBGA package

Everspin



Cypress



PIN #	Everspin	Cypress	Everspin connection	Everspin Comments
A1	DC	NC	Do not connect	Internally pulled to VIL. Prefer to float. Pulling to VIH or VIL may increase power consumption.
A6	DC	NC	Do not connect	Internally pulled to VIL. Prefer to float. Pulling to VIH or VIL may increase power consumption.
B1	NC	NC	Not connected to die.	Do not care.
B2	DC	NC	Do not connect	Internally pulled to VIL. Prefer to float. If driven, must be pulled to VIL
B6	DC	NC	Do not connect	Prefer to float. If driven, must be pulled to VIL
C2	NC	NC	Not connected to die.	Do not care.
C5	NC	NC	Not connected to die.	Do not care.
E3	DC	VCap	Do not connect	Internally pulled to VIL, prefer to float. Pulling to VIH or VIL may increase power consumption.
F2	NC	NC	Not connected to die.	Do not care.
F5	NC	NC	Not connected to die.	Do not care.
G1	NC	NC	Not connected to die.	Do not care.
G2	NC	HSB_	Not connected to die.	Do not care.
G6	NC	NC	Not connected to die.	Do not care.
H6	NC	NC	Not connected to die.	Do not care.

Table 2 - Pin function comparison between MRAM and nvSRAM, 48 FBGA package

PACKAGE COMPATIBILITY

The Everspin 44 pin TSOP2 and FBGA devices are drop in compatible with the corresponding Cypress equivalents. However, see figures 3 and 4 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical "Keep out" areas for these packages.

EVERSPIN FBGA PACKAGE

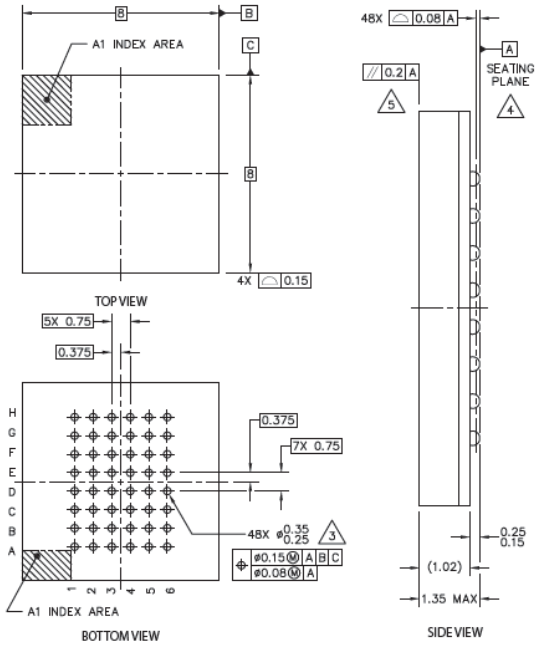


Figure 3

nvSRAM FBGA PACKAGE

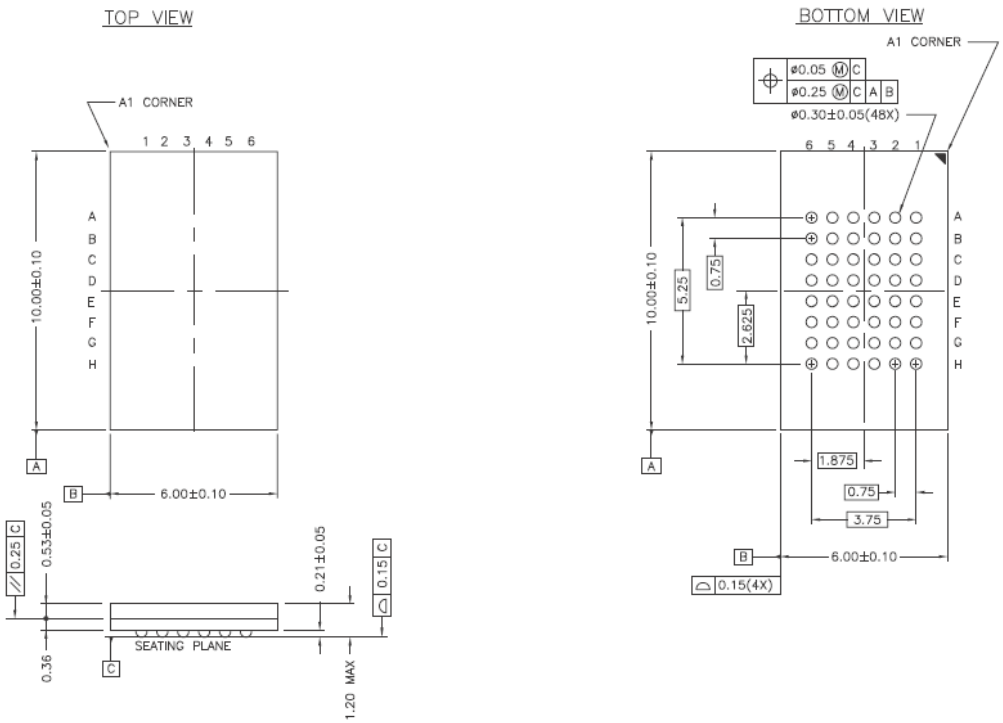


Figure 4

OTHER REPLACEMENT DESIGN CONSIDERATIONS

HSB SOFTWARE

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

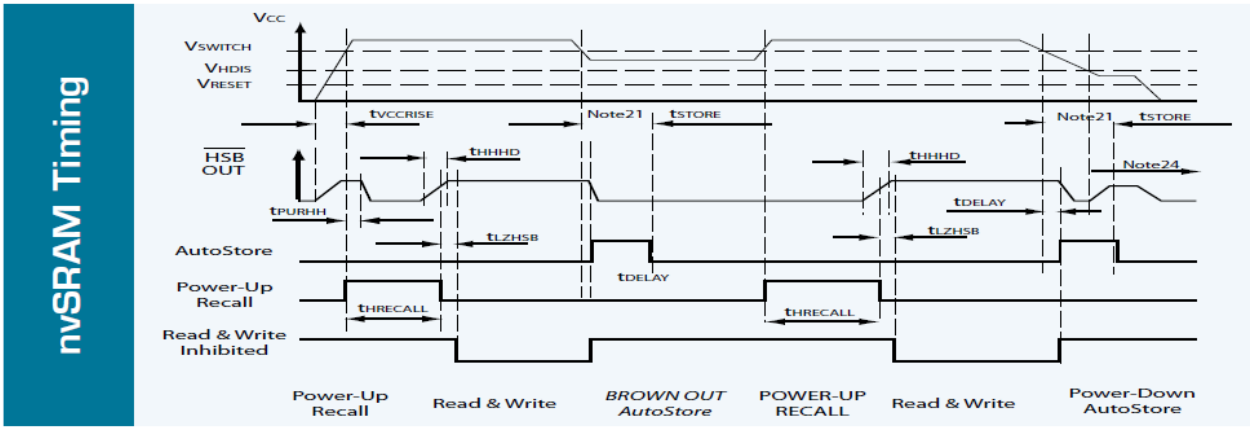
MRAM requires control signals /E and /W to track the power supply during power-up and be held high for a 2 ms start-up period a much shorter power-up requirement than the

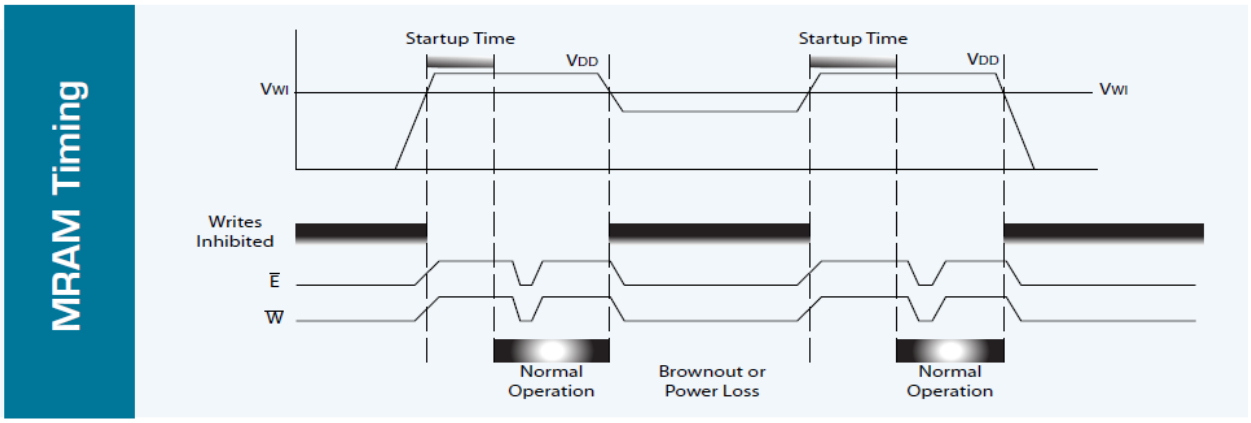
nvSRAM. When power fails, the Everspin MRAM simply inhibits write operations and no special power down timing considerations are needed since data is always non-volatile.

The nvSRAM device requires the /WE signal to track the power supply during power-up and be held high during the power-up recall period of 20 ms. The nvSRAM must sense the power failure, decouple the power supply from its backup capacitor, wait for any SRAM operations to complete, and then perform a parallel write to the EEPROM storage element during the 8 ms period after power has failed. This sequence is complicated by the fact that power falls at various ramp rates and in some cases bounces above and below the power supply threshold (brown outs) in rapid succession. Such conditions are not easily simulated or tested raising concerns about reliability of the backup storage cycle and the data in the EPROM.

POWER-UP SEQUENCING

Both MRAM and nvSRAM will operate from a standard +3.3 volt power supply with +/-10% power supply range. Both MRAM and nvSRAM have similar standby and active operating currents, however, the “Start-up” time for the MRAM is 2ms vs. 20ms for the nvSRAM. Proper decoupling capacitors should be used to assure reliable operation.





RELIABILITY CONSIDERATIONS FOR COMPARISON

CY14B104LA-xx uses conventional trapped charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles.

Everspin MRAM will provide a cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile EEPROM storage element in every cell. The total cell complexity is 12-transistors. MR2A08Axxx is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability.

The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable data retention.

MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125 °C.

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Replacing the Cypress CY14B104LA nvSRAM with Everspin MR2A08A MRAM

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