Replacing the Cypress CY62137EV30LL MoBL SRAM with Everspin's MR1A16Axxx35 MRAM

EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

OVERVIEW

The Everspin 2Mb MRAM M1A16Axxx35 can operate with the Cypress 2Mb SRAM CY62137EV30LL slower timing, but also allows the system designer to take advantage of MRAM's faster random access cycle time.
The Everspin 2Mb MRAM M1A16Axxx35 is available in 44 Pin TSOP2 as well as 48 Pin BGA packages.

BENEFITS OF MR1A16Axxx35

Upgrading to Everspin MRAM provides many benefits over Cypress SRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Standard TSOP2 and BGA package

GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin Toggle technology magnetic RAM (MRAM) is essentially non-volatile SRAM. Replacing SRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a volatile SRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source.

CONSIDERATIONS FOR REPLACING CYPRESS CY62137EV30LL (128k x 16) MoBL SRAM with EVERSPIN MR1A16Axxx35 ((128k x 16) MRAM

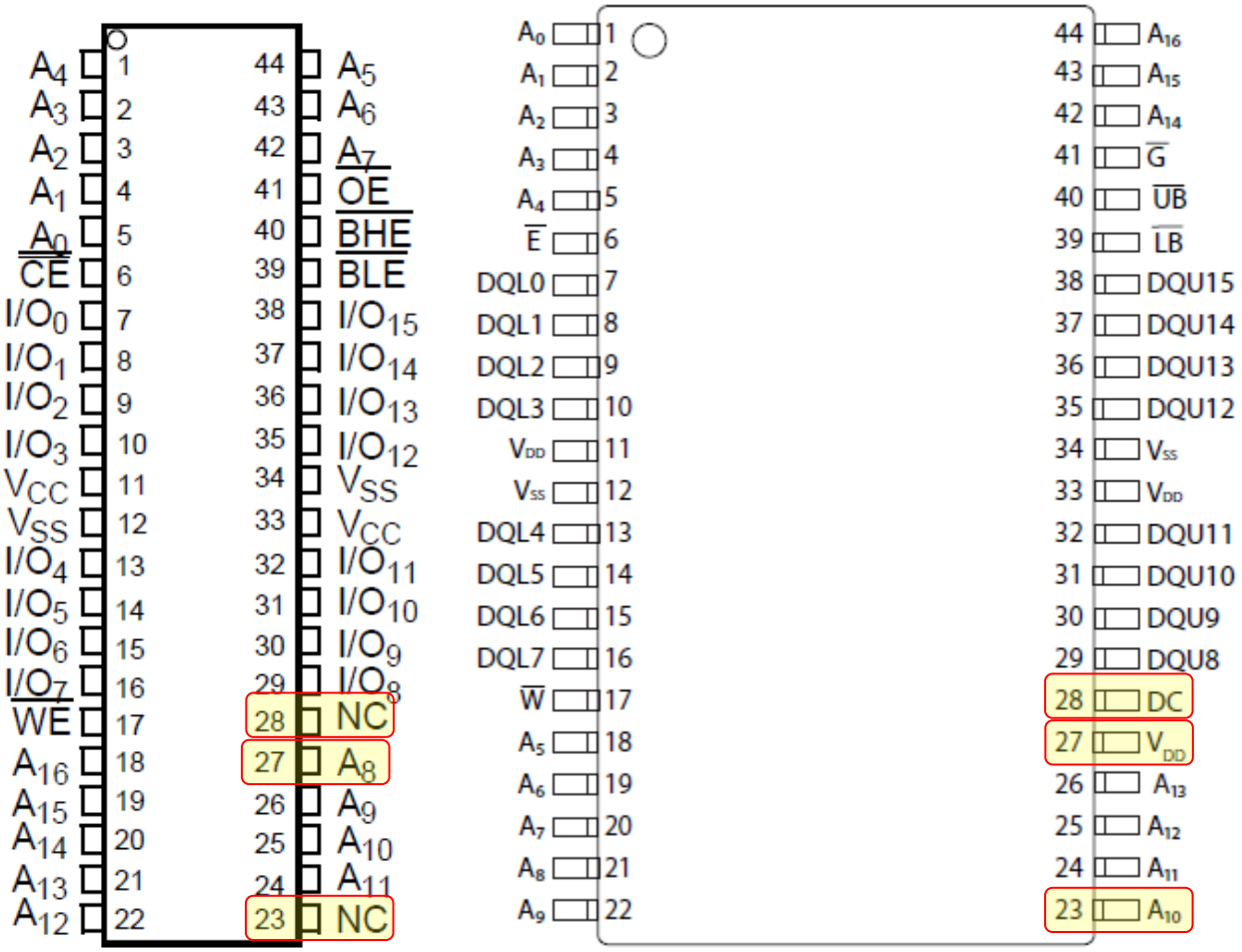
Designers considering a replacement of CY62137EV30 with MR1A16Axxx need to consider differences in package size and timing. Everspin MR1A16Axxx has a different operating voltage range from 3.0V to 3.6V, with a typical of 3.3V.

Table 1 – Overview: CY62137EV30LL-45ZSXI vs. MR1A16ACYS35

Parameter	CY62137EV30LL	MR1A16ACYS35
Package	44 PIN TSOP II	44 PIN TSOP II
Size and Height	10.2 × 18.5 × 1.2 mm	10.2 x 18.5 x 1.2 mm
Pinout / Footprint	See Figure 1 and Table 2 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	0ns Address Hold Time	12ns Minimum Address Hold Time. See Figure 7 below

Figure 1 – Pinout/Footprint Comparison and Considerations

44 PIN TSOP II



Cypress **Everspin Technologies**

Table 2 – Pin Function Comparison

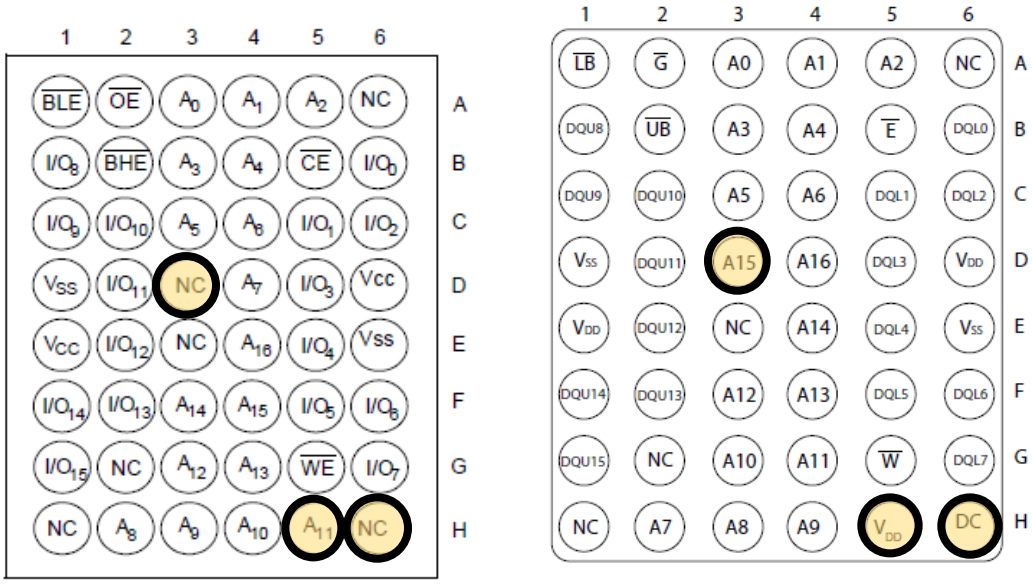
Pin #	Cypress	Everspin	Everspin Definition	Everspin Comments
23	NC	A10	Address Input	
27	A8	Vdd	Power Supply	
28	NC	DC	Do Not Connect	This pin is used for test. Prefer to float. If driven, must be pulled to VIL.

Table 3 – Overview: CY62137EV30LL-45BVXI vs. MR1A16ACMA35

Parameter	CY62137EV30	MR1A16ACMA35
Package	48 Ball VFBGA	48 Ball BGA
Size and Height	6 × 8 × 1.0 mm	10 x 10 x 1.35 mm
Pinout / Footprint	See Figure 2 and Table 4 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	0ns Address Hold Time	12ns Minimum Address Hold Time. See Figure 7 below

Figure 2 – Pinout/Footprint Comparison and Considerations

48 BALL BGA



Cypress **Everspin Technologies**

Table 4 – Pin Function Comparison

Ball #	Cypress	Everspin	Everspin Definition	Everspin Comments
D3	NC	A15	Address Input	
H5	A11	Vdd	Power Supply	
H6	NC	DC	Do Not Connect	This pin is used for test. Recommended to float. If driven, must be pulled to VIL.

PACKAGE COMPATIBILITY

The Everspin Technologies 44 Pin TSOP 2 package is a drop-in replacement with the corresponding Cypress equivalent (see Figure 3). The Everspin Technologies 48 Ball BGA package is a close-fit with the corresponding Cypress equivalent. However, see figure 4 and 6 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical "Keep out" areas for these packages. Please refer to the current datasheet for details.

Figure 3 – EVERSPIN 44-TSOP2 Package Outline

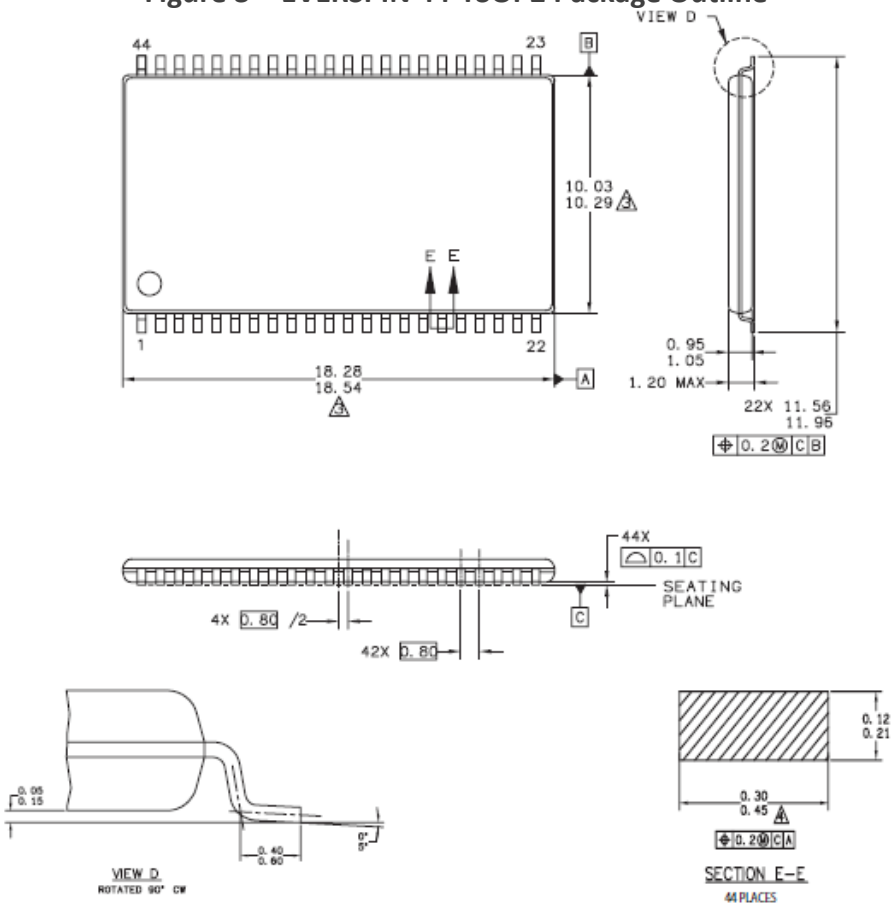


Figure 4 – EVERSPIN Package Outline 10x10mm 48-BGA

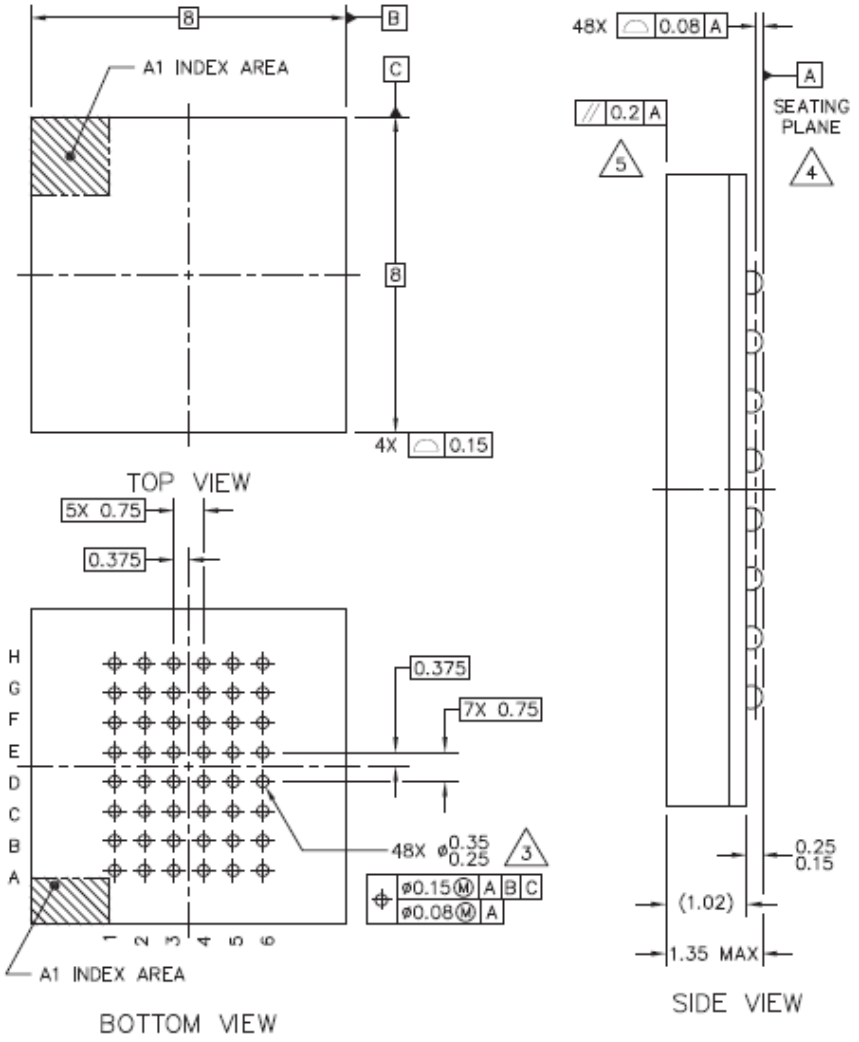


Figure 5 – Cypress 44-pin TSOP Z44-II Package Outline

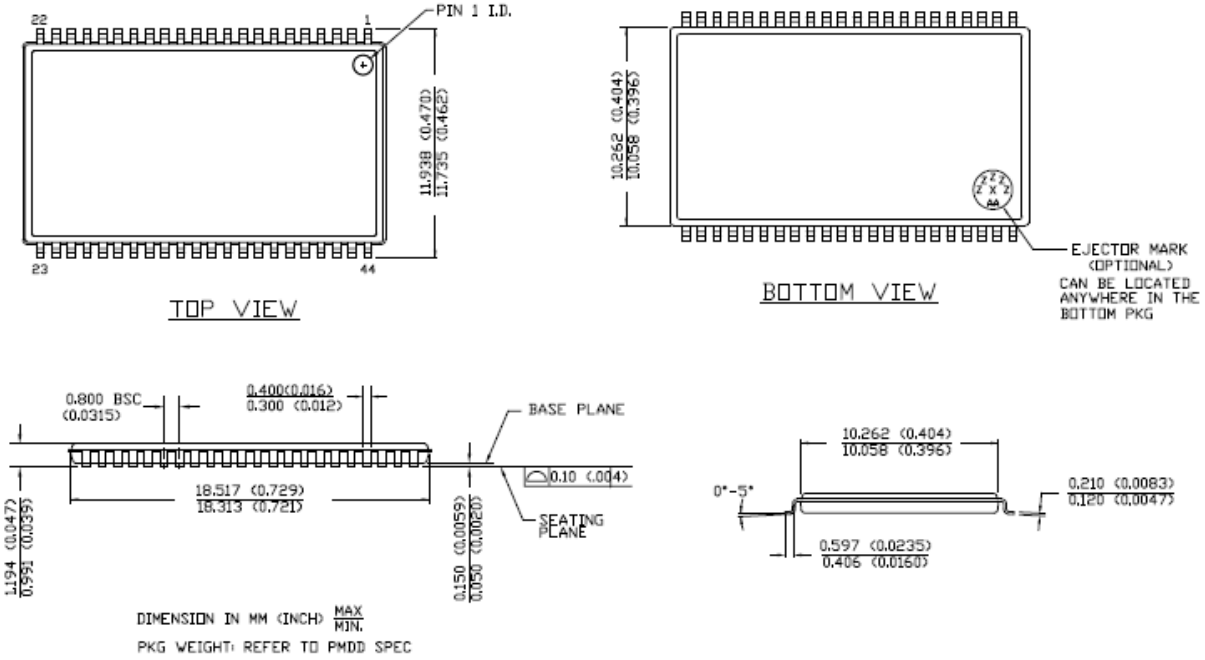
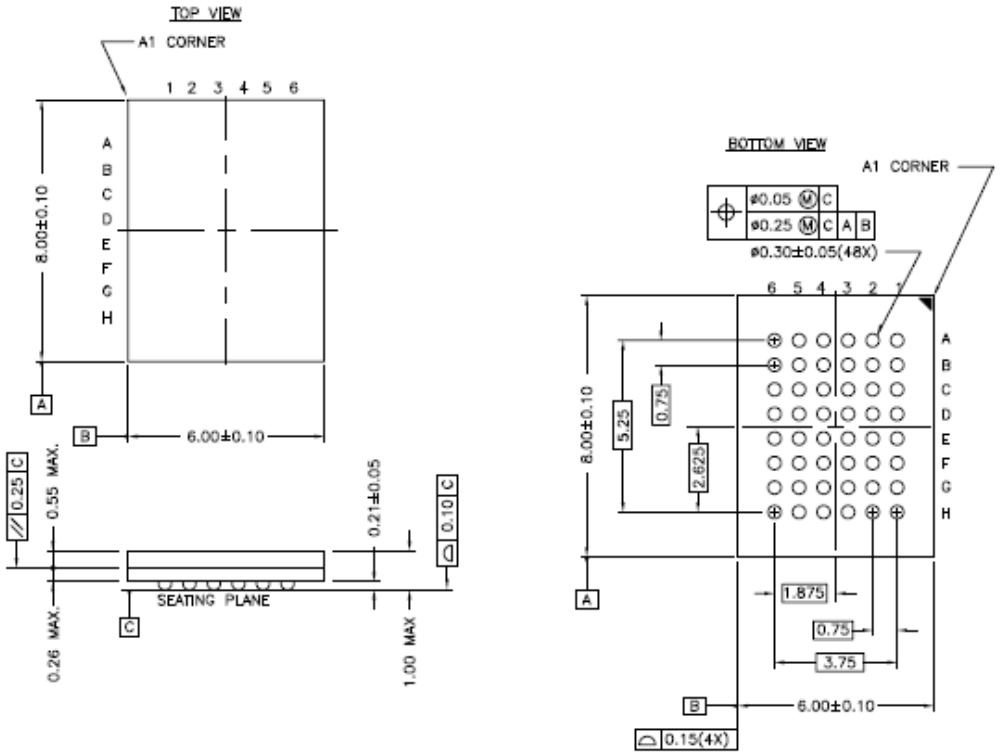


Figure 6 – Cypress Package Outline 6 x 8 x 1mm 48-VFBGA

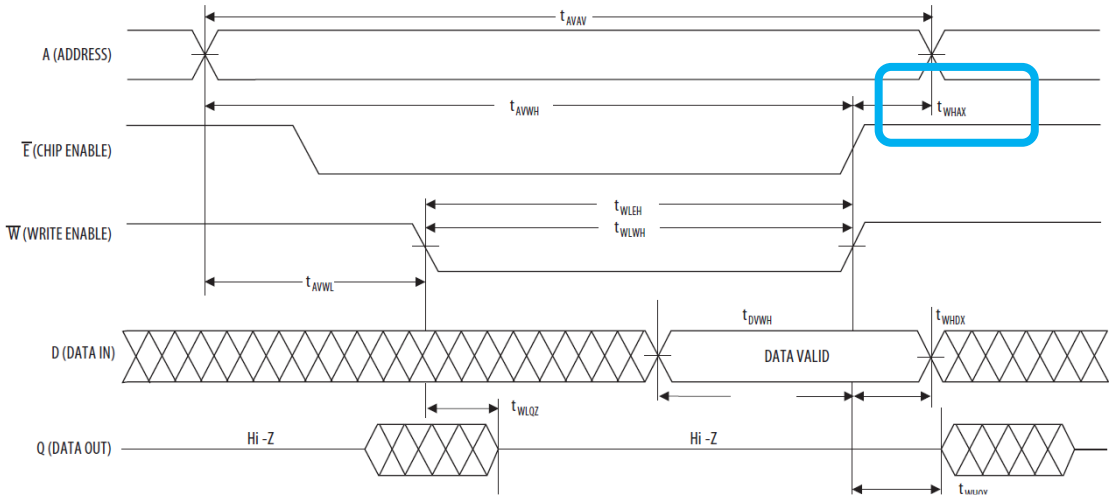


OTHER REPLACEMENT DESIGN CONSIDERATIONS

MRAM ADDRESS HOLD TIME

The Address Hold Time (Everspin Write Recovery Time, tWHAX) for the M1A16Axxx35 is a minimum of 12ns compared to 0ns minimum for CY62137EV30LL.

Figure 7 – 12ns Minimum for Address Hold Time for MR1A16Axxx35



Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the SRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the SRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

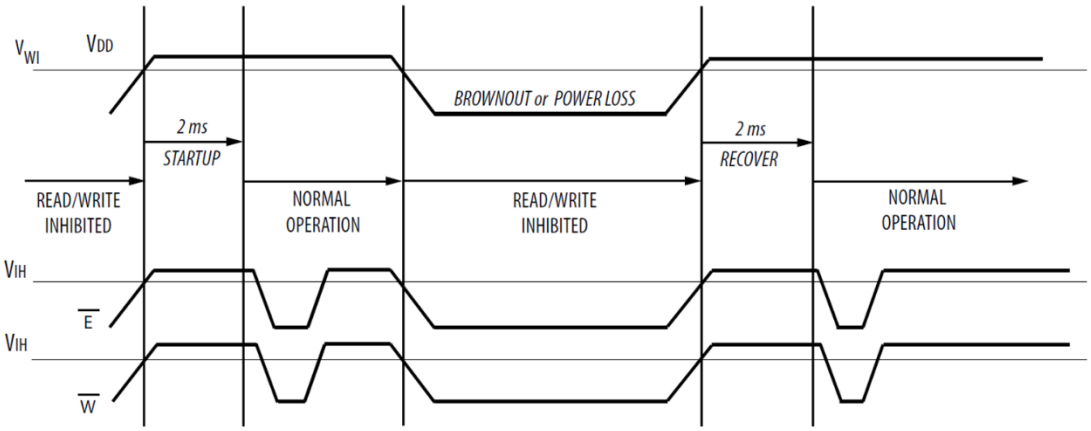
The MRAM is protected from write operations whenever VDD is less than VWI. As soon as VDD exceeds VDD(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The E and W control signals should track VDD on power up to VDD- 0.2 V or VIH (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives E and W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where VDD goes below VWI, writes are protected and a startup time must be observed when power returns above VDD(min).

MRAM POWER-UP SEQUENCING

Both MRAM and SRAM will operate from a standard +3.3 V power supply with +/-10% power supply range. Both MRAM and SRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 45ns for the SRAM. Proper decoupling capacitors should be used to assure reliable operation. The power loss/startup sequence for the MRAM is shown below:

MRAM Timing



SUMMARY

Replacing a CY62137EV30LL with Everspin's M1A16Axxx35 2Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note.

Contact Information:

Author:

Paolo Schiappacasse

FAE EMEA

Everspin Sales

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

5670 W. Chandler Road, Suite 100

Chandler, Arizona 85226

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

Everspin Technologies, Inc.