Replacing the Cypress CY62136ESL-45ZSXI MoBL SRAM with Everspin's MR1A16Axxx35 MRAM

EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

OVERVIEW

The Everspin 2Mb MRAM M1A16Axxx35 can operate with the Cypress 2Mb SRAM CY62136ESL-45ZSXI slower timing, but also allows the system designer to take advantage of MRAM's faster random access cycle time. The Everspin 2Mb MRAM MR1A16AxYS35 is available in a 44 pin TSOP2 as well as a 48 ball BGA package (option not available from Cypress).

BENEFITS OF MR1A16Axxx35

Upgrading to Everspin MRAM provides many benefits over Cypress SRAM:

- Faster Random Access Operation
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Standard TSOP2 and BGA packages

GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin's Toggle MRAM (Magnetoresistive RAM) performs essentially as non-volatile SRAM. Replacing SRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a volatile SRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source.

CONSIDERATIONS FOR REPLACING CYPRESS CY62136ESL-45ZSXI (128k x 16) MoBL SRAM with EVERSPIN MR1A16Axxx35 (128k x 16) MRAM

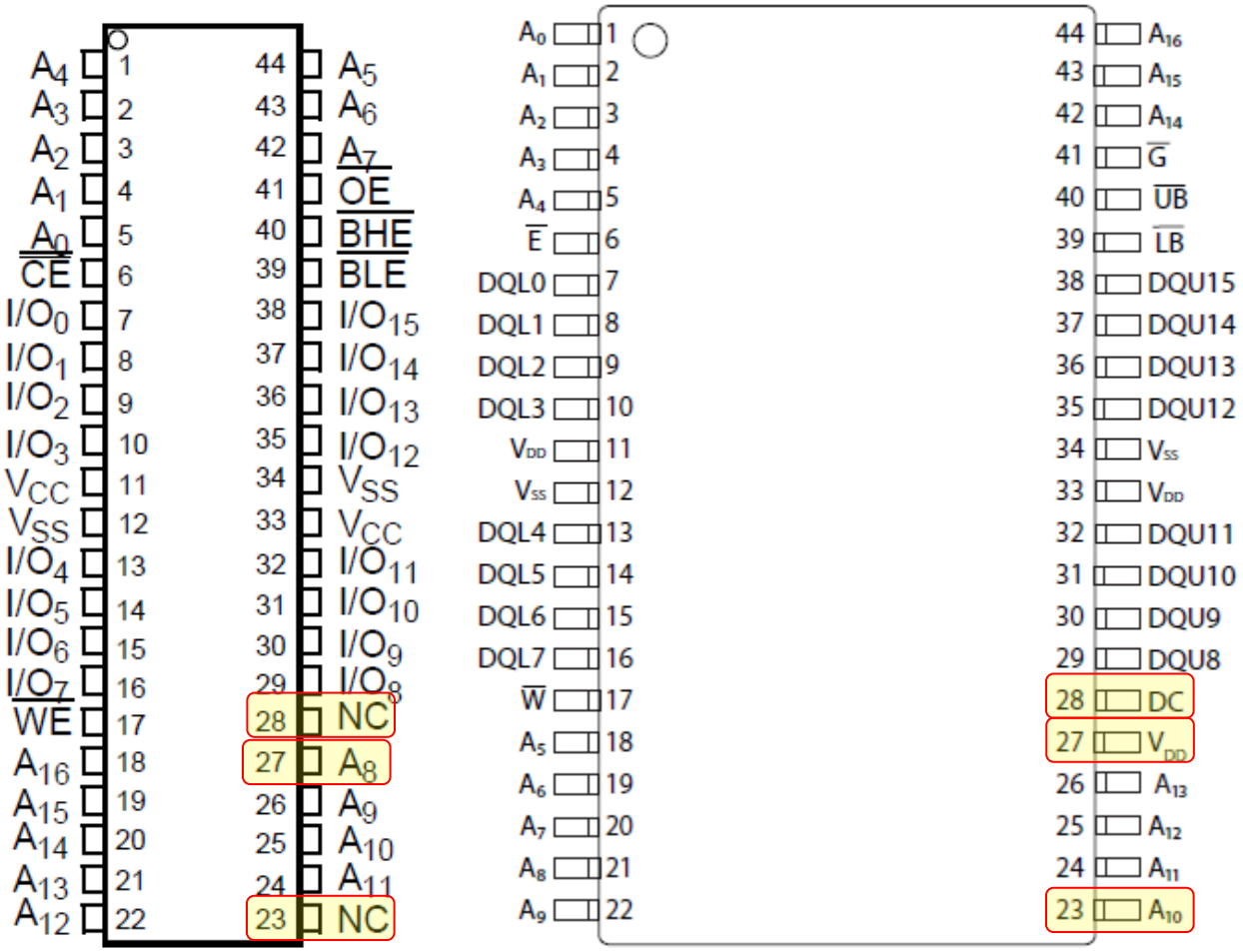
Designers considering a replacement of CY62136ESL-45ZSXI with MR1A16Axxx need to consider differences in package size, timing and power supply. Everspin MR1A16Axxx has a different operating voltage range from 3.0V to 3.6V, with a typical of 3.3V.

Table 1 – Overview: CY62136ESL-45ZSXI vs. MR1A16ACYS35

Parameter	CY62136ESL-45	MR1A16ACYS35
Package	44 PIN TSOP2	44 PIN TSOP2
Size and Height	10.2 × 18.5 × 1.2 mm	10.2 x 18.5 x 1.2 mm
Pinout / Footprint	See Figure 1 and Table 2 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	0ns Address Hold Time	12ns Minimum Address Hold Time. See Figure 7 below.

Figure 1 – Pinout/Footprint Comparison and Considerations

44 PIN TSOP2



Cypress **Everspin Technologies**

Table 2 – Pin Function Comparison

Pin #	Cypress	Everspin	Everspin Definition	Everspin Comments
23	NC	A10	Address Input	
27	A8	V_{DD}	Power Supply	
28	NC	DC	Do Not Connect	This pin is used for test. Recommend to float. If driven, must be pulled to V_{IL}.

PACKAGE COMPATIBILITY

The Everspin Technologies 44 Pin TSOP2 package is a drop-in replacement with the corresponding Cypress equivalent (see Figure 2). The Everspin Technologies 48 Ball BGA package is a different fit (see Figure 3), not available with the corresponding Cypress SRAM. Please refer to the current datasheet for details.

Figure 2 – EVERSPIN 44-TSOP2 Package Outline

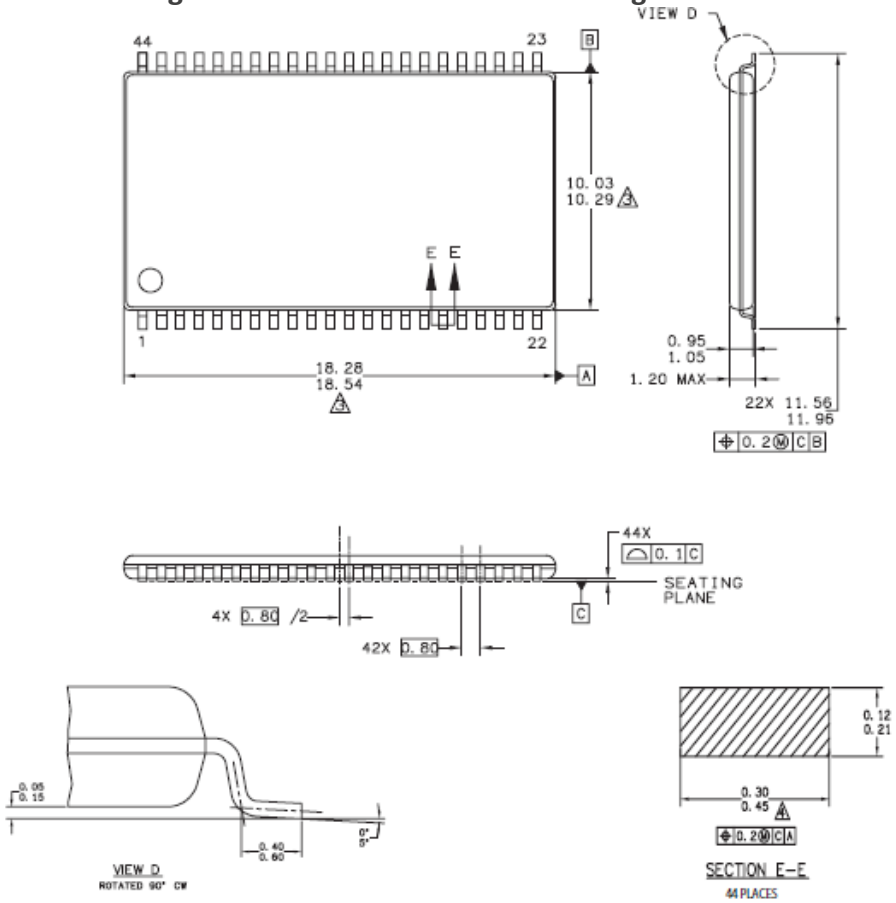


Figure 3 – EVERSPIN Package Outline 10x10mm 48-BGA

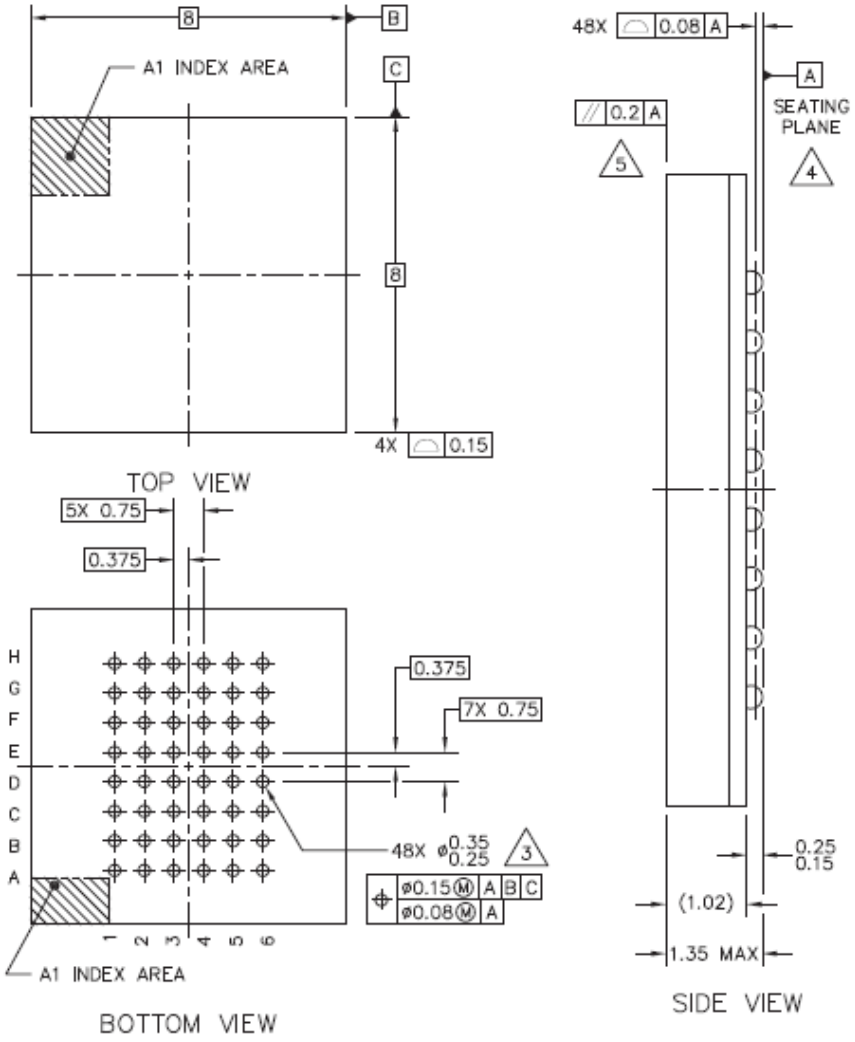
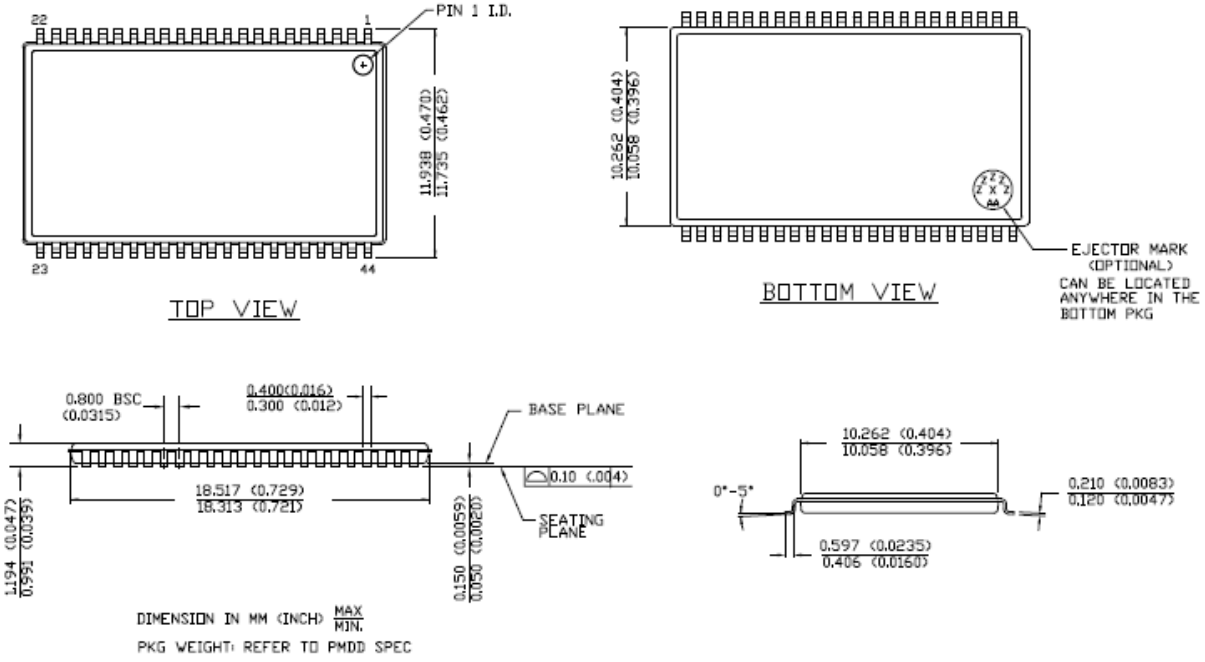


Figure 4 – Cypress 44-pin TSOP Z44-II Package Outline

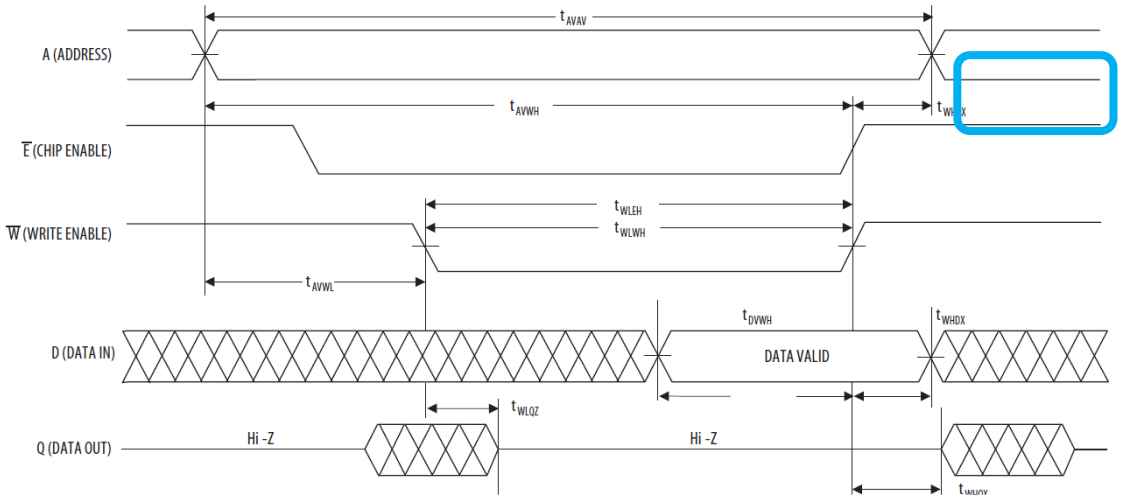


OTHER REPLACEMENT DESIGN CONSIDERATIONS

MRAM ADDRESS HOLD TIME

The Address Hold Time (Everspin Write Recovery Time, tWHAX) for the M1A16Axxx35 is a minimum of 12ns compared to 0ns minimum for CY62136ESL-45ZSXI.

Figure 5 – 12ns Minimum for Address Hold Time for MR1A16Axxx35



SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid for 20 years across the full temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

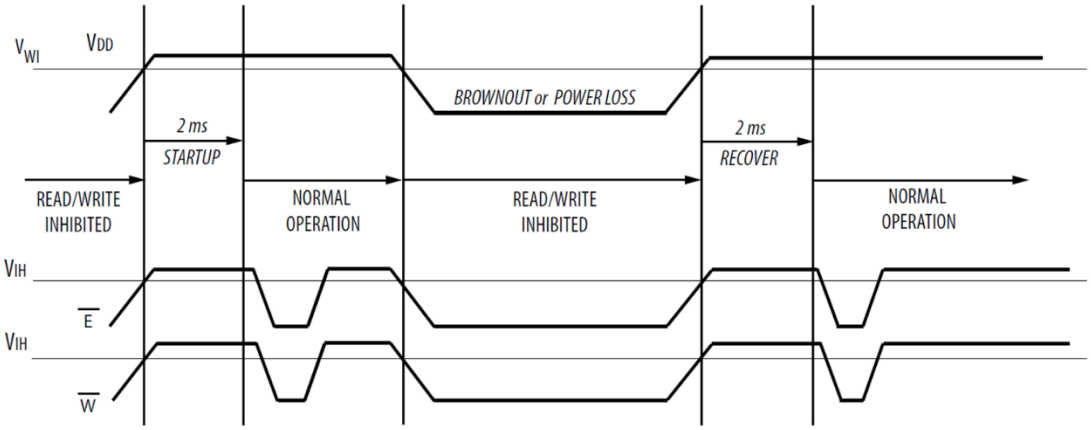
The MRAM is protected from write operations whenever V_{DD} is less than V_{WI}. As soon as V_{DD} exceeds V_{DD}(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The $\overline{E}$ and $\overline{W}$ control signals should track V_{DD} on power up to V_{DD}- 0.2 V or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives $\overline{E}$ and $\overline{W}$ should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI}, writes are protected and a startup time must be observed when power returns above V_{DD}(min).

MRAM POWER-UP SEQUENCING

Both MRAM and SRAM will operate from a standard +3.3 V power supply with at least a +/-10% power supply range. The "Start-up" time for the MRAM is 2ms. Proper decoupling capacitors should be used to assure reliable operation. The power loss/startup sequence for the MRAM is shown below:

MRAM Timing



SUMMARY

Replacing a CY62136ESL-45ZSXI with Everspin's M1A16Axxx35 2Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note.

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