

Replacing the Cypress CY15B102N-ZS60XA FRAM with Everspin MR1A16AxYS35 MRAM

EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

OVERVIEW

The Everspin 2Mb MRAM MR1A16AxYS35 can operate with the Cypress 2Mb FRAM FM28V202A-TG slower timing, but also allows the system designer to take advantage of MRAM's three times faster random access cycle time. The MR1A16AxYS35 is available in 44 Pin TSOP2 and a 48-BGA packages (option not available from Cypress)

BENEFITS OF MR1A16AxYS35

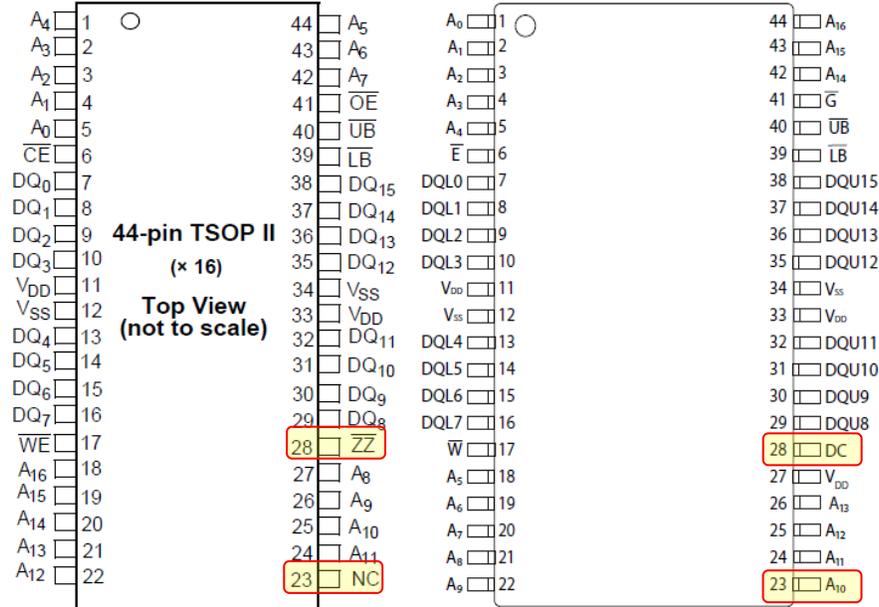
Upgrading to Everspin MRAM provides many benefits over Cypress FRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Small Footprint BGA Package

COMMON PINS

The MR1A16AxYS35 is a 2Mb non-volatile RAM organized 128Kx16 operating from a nominal 3.3V power supply and is compatible with FRAM. Both products use standard SRAM parallel address (A0-16), byte-wide bidirectional data pins (DQ0-7) and control signals (/E, /W, /G). Each can be supported by a common timing interface and will function as random access read/write memories that retain data without external battery when power is removed. Everspin does not support the /ZZ sleep function. /ZZ may require pull-up.

REPLACING CYPRESS CY15B102N-ZS60XA FRAM WITH EVERSPIN MR1A16AxYS35 MRAM



MRAM PROVIDES FASTER TIMING

The MR1A16AxYS35 and CY15B102N use address, data, and control signals that are similar to standard SRAM. The Everspin MR1A16AxYS35, however, allows for faster read and write operations at 35 ns. The Cypress FRAM requires a read cycle time of at least 90ns for random read accesses. The internal operation of the CY15B102N requires a precharge time of at least 30ns following a 60ns initial read access, resulting in a random access minimum cycle time of 90ns. The pre-charge time is present whether self-timed by the part or initiated by the user by bringing /CE high. FRAM performs the read during the initial access portion of the cycle time and then restores the data to the memory cell (writes data back) during the pre-charge time like a DRAM. This is known as destructive readout operation. MRAM can operate with this slower FRAM read sequence but MRAM is actually much faster as it does not have a destructive read mechanism. Both read and write cycles wear out the FRAM. MRAM has unlimited read and write endurance. The MR1A16AxYS35 supports a 35-ns read access and cycle time. The MR1A16AxYS35 does not require a precharge cycle and is two times faster than the FRAM on initial read access time and three times faster on random accesses. The FRAM requires 90ns to complete a write cycle just as it does a read cycle. The MRAM will operate with this timing but actually has a write cycle time of just 35 ns (3 times faster than FRAM). To take advantage of the three times faster random read and write speed of the MR1A16AxYS35, you may wish to modify the control interface. MRAM plugs directly into most SRAM controllers without change.

POWER CYCLING CONSIDERATIONS

The CY15B102N has a power startup time of 1 ms while the MR1A16AxYS35 is specified at 2 ms. This difference in startup times will not be an issue in most system designs since the power-up master reset is purposely made much longer to assure that all circuitry is stabilized for start of operation.

POWER SUPPLY CONSIDERATIONS

Both the MRAM and the FRAM are specified at nominal 3.3V power supply. The FRAM has a standby current of 150 uA. To enable three times faster random access speed, MRAM's standby current is 9 mA. For battery-powered applications, designers can take advantage of MRAM's non-volatility and power gate the MRAM to reduce standby power to zero when not in use.

REPLACING CYPRESS CY15B102N-ZS60XA FRAM
WITH EVERSPIN MR1A16AxYS35 MRAM**READ AND WRITE CURRENTS**

The read and write current for the MR1A16AxYS35 is similar to the CY15B102N at 12 mA active current for 105 ns cycle time. MR1A16AxYS35 is specified at 80 mA read, 165 mA write when operating at its faster 35 ns cycle time operation.

RELIABILITY CONSIDERATIONS FOR COMPARISON

The CY15B102N FRAM architecture employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation has to restore the polarization to its original state after the initial read which adds cycle time to the read operation. FRAM Read and Write cycles require an initial "Pre-charge" time which can increase the initial access time. Ambient operating temperatures above 85°C accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM will provide the most cost-effective non-volatile RAM solution. MR1A16A MRAM is built using a much simpler 1-transistor, 1-magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability. MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. Data retention is better than 20 years at 125°C.

SUMMARY

Replacing a CY15B102N with Everspin's MR1A16AxYS35 2Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note.

REPLACING CYPRESS CY15B102N-ZS60XA FRAM WITH EVERSPIN MR1A16AxYS35 MRAM

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