SOIC PACKAGE

16-pin SOIC

- Compliant with RoHS, REACH regulations and practices.
- Contain no Red Phosphorus.
- Lead Free.
- All products meet MSL-3 moisture sensitivity level.
- Standard Reflow profile.
- Compatible with similar low-power SRAM products and other nonvolatile RAM products.

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COMPLIANCE WITH ENVIRONMENTAL REGULATIONS AND DIRECTIVES

Table 1 – Environmental Regulation and Directive Compliance

Environment	Statement Summary	Download Full Statement
ISO9001:2008	Everspin Technologies is in conformance with ISO9001:2008	Certificate
RoHS Directives	Statement of RoHS 1 and the recast Directive 2011/65/EU is commonly referred to as RoHS 2 Compliance. Everspin MRAM products are also "halogen-free".	Full Statement
REACH Regulations	REACH regulations require article suppliers to inform recipients if an article contains a Substance of Very High Concern (SVHC) in excess of 0.1% by weight. Based on the material content certifications provided by Everspin's suppliers, none of these substances are present in the materials we use in our products, including packing and shipping materials.	Full Statement
Red Phosphorus	Everspin Technologies, Inc. MRAM products do not contain Red Phosphorus CAS# 7723-14-0 as an intentional additive.	Full Statement

MULTIPLE REFLOW CYCLES AND MOISTURE RESISTANCE

All Everspin packages are qualified by the procedure defined in IPC/JEDEC joint specification IPC/JEDEC J-STD-020D.1. They are guaranteed to withstand up to three reflow cycles without permanent damage, provided the conditions for the rated moisture resistance level for the part are observed prior to reflow.

Everspin parts are generally rated for MSL Level 3. Exceptions may exist and are noted in their respective data sheet. Please the check the latest individual product data sheet to confirm the rated MSL for the product.

RECOMMENDED REFLOW TEMPERATURES AND TIMING

Everspin products can be assembled using a standard assembly lead-free reflow profile. The profile below is based on IPC/JEDEC J-STD-020D.1.

Figure 1 – JEDEC J-STD-020D.1 Assembly Reflow Profile

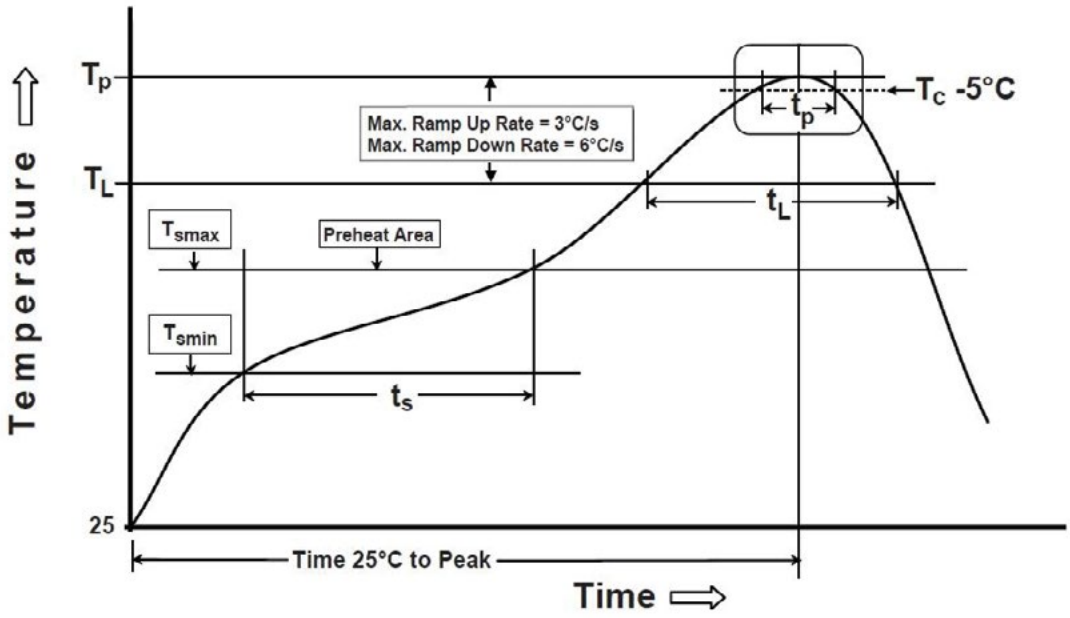


Table 2 – Recommended Reflow Times and Temperatures - All Packages

Profile Step	Parameter	Symbol	Time/Temp	Unit
Preheat / Soak	Temperature mininumum	T_{SMIN}	150	°C
	Temperature maximum	T_{SMAX}	200	°C
	Soak Time	t_S	60 - 120	Seconds
Ramp Up	Rate from T_L to T_P	T_L to T_P	3° / Sec Max	° / Sec
	25°C to T_P		8 minutes max	Minutes
Reflow	Liquidous Temperature	T_L	217	°C
	Time Above T_L		60 - 150	Seconds
	Peak Package Body Temperature	T_P	260	°C
	Time within 5° of Peak Package Body Temperature		20 - 40	Seconds
Ramp Down	Rate from T_P to T_L	T_P to T_L	6° / Sec Max	° / Sec

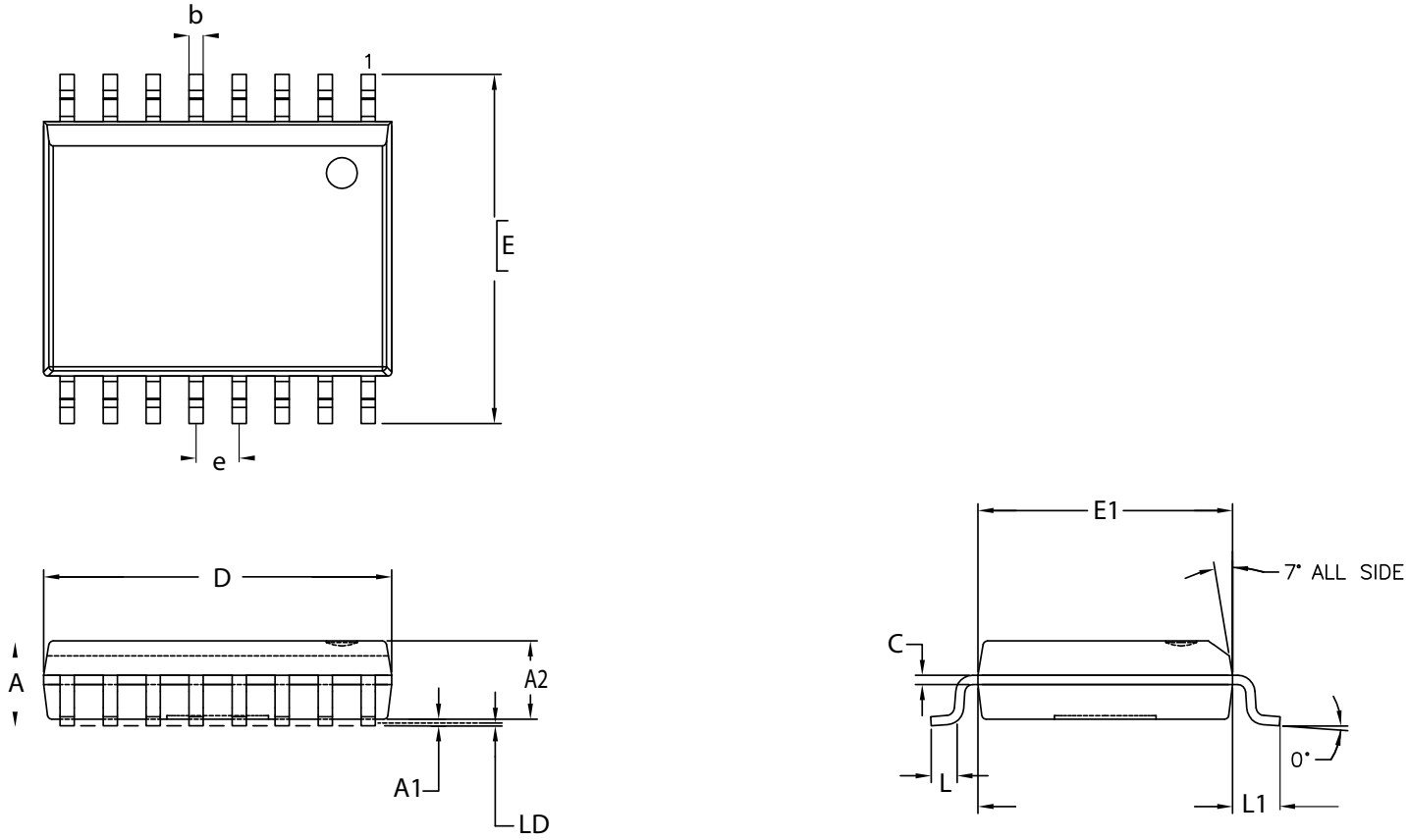
THERMAL RESISTANCE

Table 3 – Thermal Resistance 16-pin SOIC

Velocity (m/s)	T_A (°C)	Power (W)	T_J Max °C	Θ_{JA} (°C/W)	Θ_{JB} (°C/W)	Θ_{JC} (°C/W)	Ψ_{JB} (°C/W)	Θ_{JT} (°C/W)
0	25	0.792	71.0	58.1	30.6	31.6	2.0	30.6
1			64.5	49.9			2.8	29.6
2			62.8	47.7			3.2	29.1
3			61.8	46.4			3.5	28.8

PACKAGE OUTLINE DRAWINGS

Figure 2 – Package Outline 16-pin SOIC



Symbol	JEDEC MS - 013 (AA) issue (mm)			Everspin POD 16L SOIC PKG OUTLINE DWG. 300 MIL (mm)		
Ref	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	2.65	2.46	2.56	2.64
A1	0.10	-	0.30	0.127	0.22	0.29
A2	2.05	-	-	2.29	2.34	2.39
b	0.31	-	0.51	0.35	0.41	0.51
c	0.20	-	0.33	0.23	0.25	0.32
D	10.30 BSC			10.21	10.34	10.46
E	10.30 BSC			10.16	10.31	10.63
E1	7.50 BSC			7.44	7.52	7.59
L	0.40	-	1.27	0.61	0.81	1.02
L1	1.40 REF			N/A		
e	1.27 BSC			1.27 BSC		
Θ	0°	-	8°	0°	5°	8°

REVISION HISTORY

Revision	Date	Description of Change
1.0	Oct 7, 2013	Initial release
1.1	Oct 21, 2014	Added Reflow Cycle and Moisture Resistance section.
1.2	February 24, 2015	Added matte Sn plating thickness.
2.0	August 6, 2015	Removed 32-SOIC Package. Reference PCN 02895.
2.1	December 1, 2017	Updated package dimension table and drawing in Figure 2
2.2	March 22, 2018	Contact information table updated

CONTACT US

Home Page:

www.everspin.com

World Wide Information Request

WW Headquarters - Chandler, AZ

5670 W. Chandler Blvd., Suite 100

Chandler, Arizona 85224

Tel: +1-877-480-MRAM (6726)

Local Tel: +1-480-347-1111

Fax: +1-480-347-1175

support@everspin.com

Europe, Middle East and Africa

Everspin Europe Support

support.europe@everspin.com

Japan

Everspin Japan Support

support.japan@everspin.com

Asia Pacific

Everspin Asia Support

support.asia@everspin.com

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Everspin Technologies, Inc.